IN THE CLAIMS:

Kindly replace the claims with the following:

1. (Currently amended) A data processing system which is adapted to function in a reduced-power mode, comprising:

a first data processing unit that has access to a memory belonging to the first data processing unit: and,

a second data processing unit having its own memory, said second data processing unit having access to the memory belonging to the first data processing unit, wherein the first data processing unit is arranged for offering the second data processing access to the memory belonging to the first data processing unit in a reduce-power mode of the data processing system so that the second data processing unit utilizes the memory belonging to the first data processing unit instead of its own switched-off memory.

2. (Previously presented) The data processing system as claimed in Claim 1, wherein the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a period of time in which the reduced-power mode of the data processing system implies a reduced-power mode of the first data processing unit.

3. (Currently amended) [[The]] A data processing system ~~which may be~~ situated in a reduced-power mode, comprising:

a first data processing unit that has access to a memory belonging to the first data processing unit, wherein the first data processing unit is arranged for offering [[the]] a second data processing unit access to the memory belonging to the first data processing unit ~~in a reduced-power mode of the first data processing system~~, and wherein the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit when a memory belonging to the second data processing unit is switched off.

4. (Previously presented) The system as claimed in Claim 1, wherein the memory belonging to the first data processing unit forms part of the first data processing unit.

5. (Previously presented) The system as claimed in Claim 1, wherein the memory belonging to the first data processing unit is a cache memory.

6. (Previously presented) The system as claimed in Claim 1, wherein the first data processing unit is a microprocessor.

7. (Previously presented) The system as claimed in Claim 1, wherein the second data processing unit is a video controller.

8. (Currently amended) A data processing unit having access to a memory belonging to the data processing unit situated in a switched-off mode, wherein the memory belonging to the data processing unit is accessible to a second data processing unit, the second data processing unit further having access to a second memory unit which is switched off~~of its own~~.

9. (Currently amended) The data processing ~~system~~ unit as claimed in Claim 8, further comprising:

a mechanism that allows the [[first]] data processing unit to offer the second data processing unit access to the memory belonging to the [[first]] data processing unit ~~in the reduced-power mode~~.

10. (Currently amended) The data processing ~~system~~ unit as claimed in Claim 9, wherein the second memory unit can be accessed by system components other than the ~~first~~ data processing unit or the second data processing units ~~in the reduced-power mode~~.

11. (Currently amended) [[The]] A data processing unit having access to a memory belonging to the data processing unit that may be situated in a reduced-power

mode, ~~wherein the data processing unit is arranged for offering access in the reduced-power mode to the memory belonging to the data processing unit~~,

a mechanism that allows the first data processing unit to offer a second data processing unit access to the memory belonging to the first data processing unit in the reduce-power mode, wherein the first processing unit is arranged for offering the second data processing unit access to the first memory when the second memory is switched off.

12. (Currently amended) The data processing ~~system~~ unit as claimed in Claim 9, wherein the memory belonging to the ~~first~~ data processing unit is a cache memory.

13. (Currently amended) A data processing system that may be situated in a reduced-power mode having a first data processing unit that has access to a first memory associated with the first data processing unit and a second data processing unit that has access to the first memory, said system comprising:

a second memory operating in a switched-off state associated with the second data processing unit; and

a mechanism that allows the first data processing to offer the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system so that the second data processing unit does not access the second memory during reduced power mode when the first memory can service the second data processing unit.

14. (Previously presented) The data processing system as claimed in Claim 13, wherein the second memory unit can be accessed by system components other that the first or second data processing units in the reduced-power mode.

15. (Previously amended) A data processing system which may be situated in a reduced-power mode having a first data processing unit that has access to a first memory associated with the first data processing unit and a second data processing unit that has access to the first memory comprising:

a second memory associated with the second data processing unit; and

a mechanism that allows the first data processing unit to offer the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system, wherein the first data processing unit is arranged for offering the second data processing unit access to the first memory when the second memory is switched off.

16. (Currently amended) The system as claimed in Claim ~~13~~ 15 wherein the memory belonging to the first data processing unit forms part of the first data processing unit.

17. (Currently amended) The system as claimed in Claim ~~13~~ 15, wherein the memory belonging to the first data processing unit is a cache memory.

18. (Currently amended) The system as claimed in Claim ~~13~~ 15, wherein the first data processing unit is a microprocessor.

19. (Currently amended) The system as claimed in Claim ~~13~~ 15, wherein the second data processing unit is a video controller.

20. (Currently amended) A data processing [[unit]] configuration comprising:

a first processor in communication with a memory, the first processor operating in a reduced-power mode and accessing a selected portion of [[the]] a first memory; and

a ~~second processor~~ video controller arranged to access ~~the unused portion~~ unselected portions of the first memory belonging to the first processor, the ~~second processor~~ video controller further assessing a second memory associated with the video controller ~~having its own memory~~.

21. (Currently amended) The data processing [[unit]] configuration as claimed in claim 20, wherein the first processor is switched-off.

22. (Currently amended) The data processing [[unit]] configuration as claimed in claim 20, wherein the ~~second processor~~ video controller [[memory]] is inhibited from accessing the second memory ~~is not accessible to the second processor~~.

23. (Currently amended) The data processing [[unit]] configuration as claimed in claim 22, wherein the ~~second processor~~ video controller ~~memory~~ is disconnected from the second memory.

24. (Currently amended) The data processing [[unit]] configuration as claimed in claim 22, wherein an energy supply to the ~~second processor~~ video controller memory is interrupted.